1. (Previously Presented) A shallow trench isolation structure in a substrate, said shallow trench isolation structure comprising:

a trench in said substrate;

a nitride liner recessed within said trench and the nitride liner forming a partially enclosed volume, said partially enclosed volume being completely filled with a dielectric material which also completely fills the trench;

wherein said nitride liner is recessed such that an uppermost surface of said nitride liner is recessed to a first depth that is greater than a transistor channel depth, Dc, of a transistor that is disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor;

the dielectric material including an oxide disposed above said nitride liner such that said oxide extends above the uppermost surface of said nitride liner to substantially a top surface of said substrate, such that substantially no polysilicon material is disposed within the trench.

2. (Original) A shallow trench isolation structure as recited in claim 1, wherein said transistor is a P-FET transistor.

3. (Previously Presented) A shallow trench isolation structure in a substrate as recited in claim 1, wherein the uppermost surface of said nitride liner is recessed to a first depth that is greater than about 1000 angstroms below a top surface of said substrate.

4. (Original) A shallow trench isolation structure in a substrate as recited in claim 1, further comprising:

an oxide layer disposed within the trench, said oxide layer underlying said nitride liner;

and

an oxide fill disposed above said nitride liner such that the nitride liner is encapsulated by the oxide fill and oxide layer.

5. (Original) A shallow trench isolation structure in a substrate as recited in claim 4, wherein the oxide fill extends above said uppermost surface of said nitride liner, substantially to a top surface of said substrate, such that substantially no void exists above said uppermost surface of said nitride liner.

6. (Canceled)

7. (Previously Presented) A shallow trench isolation structure in a substrate as recited in claim 4, wherein the oxide fill includes tetraethylortosilicate.

8-11. (Canceled)

12-23. (Canceled)

24. (Previously Presented) A shallow trench isolation structure for preventing hot carrier effects due to charge trapping, said shallow trench isolation structure comprising:

a trench in the substrate;

an oxide liner formed lining the trench and a top surface of the substrate;

a nitride liner recessed within said trench and the nitride liner forming a partially enclosed volume, said partially enclosed volume being completely filled with a dielectric material which also completely fills the trench;

wherein said nitride liner is recessed such that an uppermost surface of said nitride liner is recessed to a first depth that is greater than a transistor channel depth, Dc, of a transistor that is disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor;

an oxide fill disposed above said nitride liner, such that said oxide fill extends above and below the uppermost surface of said nitride liner substantially to a top surface of said substrate and completely filling below the uppermost surface, respectively; and

the oxide fill is disposed above said nitride liner such that polysilicon material used in other processing is prevented from entering the trench.

25. (Previously Presented) The structure of claim 24, wherein the oxide fill includes tetraethylortosilicate.